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*Gloster, C., Jr.; Subramanian, S.;*

ASIC Conference and Exhibit, 1994. Proceedings., Seventh Annual IEEE International , 19-23 Sept. 1994

Pages:366 - 369

[\[Abstract\]](#)   [\[PDF Full-Text \(264 KB\)\]](#)   IEEE CNF

#### 2 A novel scan architecture for power-efficient, rapid test [sequential circuits]

*Sinanoglu, O.; Orailoglu, A.;*

Computer Aided Design, 2002. ICCAD 2002. IEEE/ACM International Conference on , 10-14 Nov. 2002

Pages:299 - 303

[\[Abstract\]](#)   [\[PDF Full-Text \(450 KB\)\]](#)   IEEE CNF

#### 3 Static test compaction for full-scan circuits based on combinational test sets and non-scan sequential test sequences

*Pomeranz, I.; Reddy, S.M.;*

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*Sankaralingam, R.; Toubia, N.A.;*

Electronic Design, Test and Applications, 2002. Proceedings. The First IEEE International Workshop on , 29-31 Jan. 2002

Pages:159 - 163

[\[Abstract\]](#)   [\[PDF Full-Text \(266 KB\)\]](#)   IEEE CNF

#### 5 Reducing power dissipation during test using scan chain disable

*Sankaralingam, R.; Pouya, B.; Toubia, N.A.;*

VLSI Test Symposium, 19th IEEE Proceedings on. VTS 2001 , 29 April-3 May 2001

Pages:319 - 324

[\[Abstract\]](#)   [\[PDF Full-Text \(536 KB\)\]](#)   IEEE CNF

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*Ichino, K.; Asakawa, T.; Fukumoto, S.; Iwasaki, K.; Kajihara, S.;*  
Test Symposium, 2001. Proceedings. 10th Asian , 19-21 Nov. 2001  
Pages:379 - 384

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**7 Improving the test quality for scan-based BIST using a general test application scheme**

*Huan-Chih Tsai; Kwang-Ting Cheng; Bhawmik, S.;*  
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**8 Full scan fault coverage with partial scan**

*Xijiang Lin; Pomeranz, I.; Reddy, S.M.;*  
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Pages:468 - 472

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**9 A partial scan methodology for testing self-timed circuits**

*Khoche, A.; Brunvand, E.;*  
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**10 Hypertasking: automatic array and loop partitioning on the iPSC**

*Baber, M.;*  
System Sciences, 1991. Proceedings of the Twenty-Fourth Annual Hawaii  
International Conference on , Volume: ii , 8-11 Jan. 1991  
Pages:438 - 447 vol.2

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